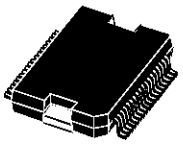
SGS-THOMSON MICROELECTRONICS

L6258

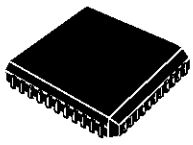
PWM CONTROLLED - HIGH CURRENT DMOS UNIVERSAL MOTOR DRIVER

PRODUCT PREVIEW

- ABLE TO DRIVE BOTH WINDINGS OF A BIPOLAR STEPPER MOTOR OR TWO DC MOTORS
- OUTPUT CURRENT UP TO 1.5A EACH WINDING
- WIDE VOLTAGE RANGE: 10V TO 45V
- FOUR QUADRANT CURRENT CONTROL, IDEAL FOR MICROSTEPPING AND DC MOTOR CONTROL
- VERY ACCURATE BUILT IN PWM CONTROL
- NO NEED FOR RECIRCULATION DIODES
- CROSS CONDUCTION PROTECTION
- THERMAL SHUTDOWN



PowerSO36



PLCC44

ORDERING NUMBERS: L6258(PowerSO36)
L6258A(PLCC44)

DESCRIPTION

L6258 is a dual full bridge for motor control applications realized in BCD technology, which is able to drive both windings of a bipolar stepper motor or bidirectionally control two DC motors.

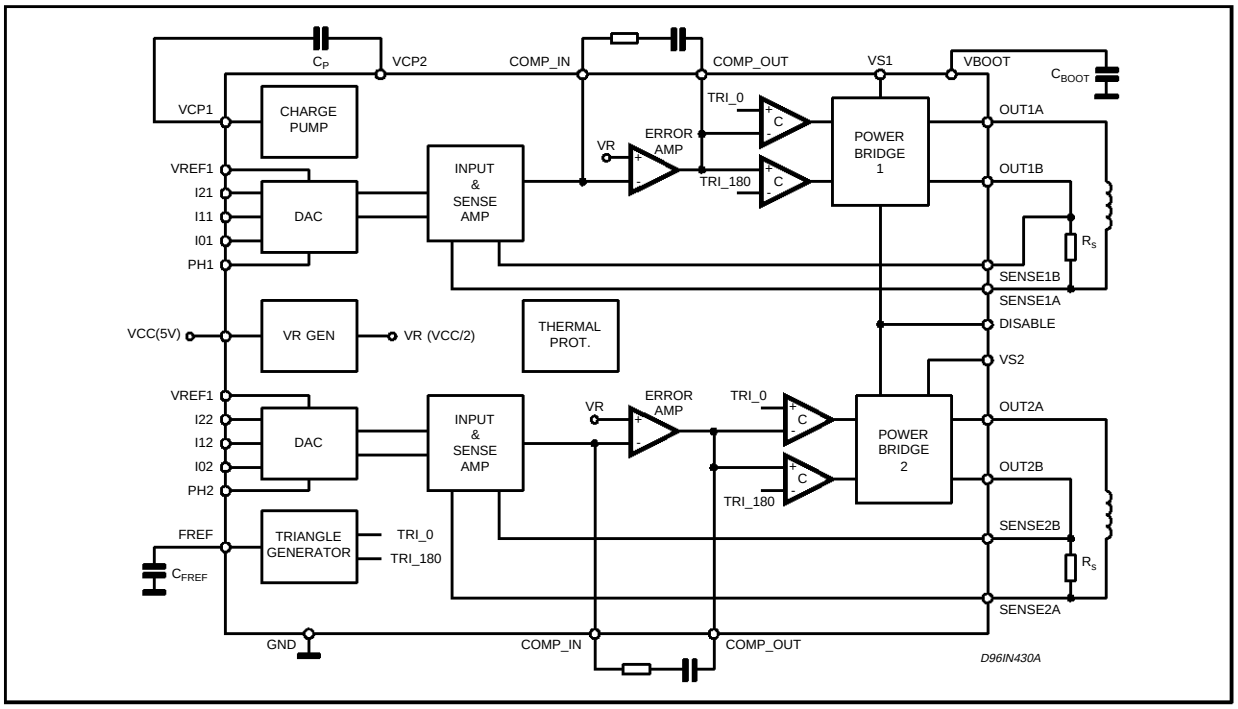
L6258 and few external components form a complete control and drive circuit for any kind of motor: it's high efficiency phase shift chopping allows a very low current ripple at the lowest current control levels, and makes this device ideal for steppers as well as for DC motors.

The logic inputs are TTL/CMOS compatible.
The power stage is a dual DMOS full bridge capable of sustaining up to 45V, and includes the diodes for current recirculation.

The output current capability is 1.5A per winding in continuous mode, with peak start-up current up to 2 A.

A thermal protection circuitry disables the outputs if the chip temperature exceeds the safe limits.

BLOCK DIAGRAM

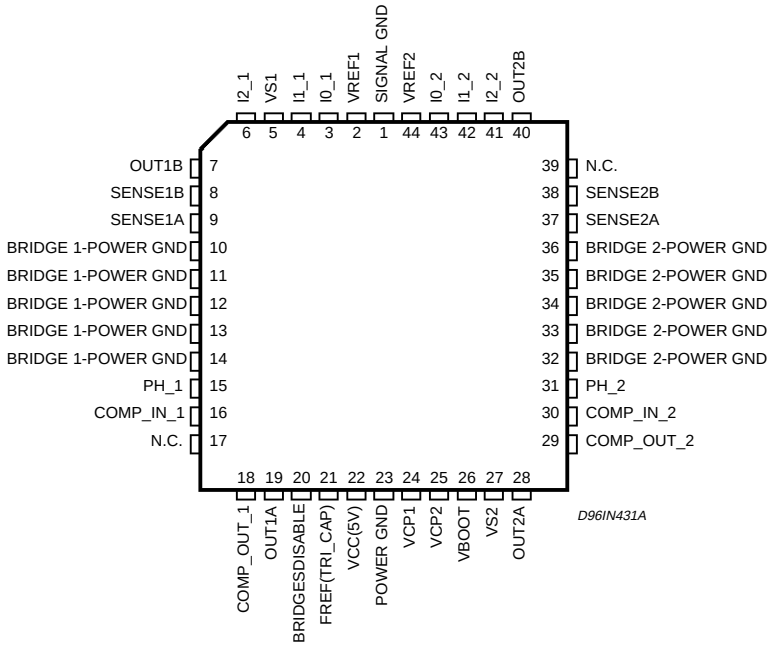


ABSOLUTE MAXIMUM RATINGS

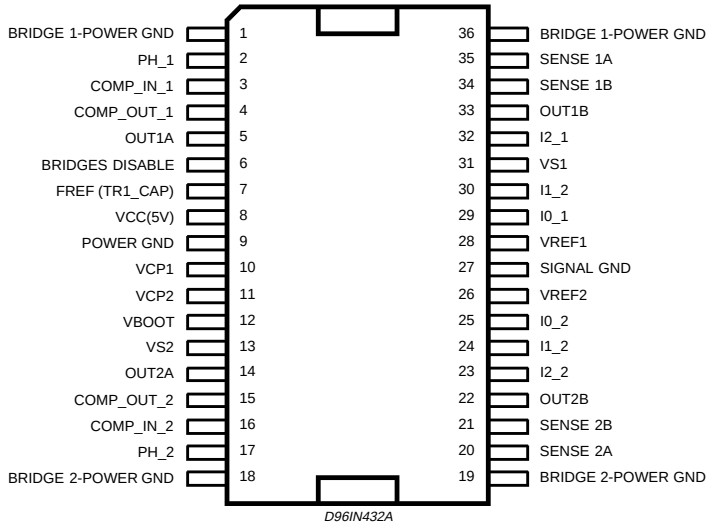
Symbol	Parameter	Value	Unit
Vs	Supply Voltage	50	V
V_{CC}	Logic Supply Voltage	7	V
I_O	Output Current (peak)	2	A
I_O	Output Current (continuous)	1.5	A
V_{in}	Logic Input Voltage Range	-0.3 to 7	V
V_{boot}	Bootstrap Supply	60	V
T_j	Junction Temperature	150	°C
T_{op}	Junction Temperature	150	°C
T_{stg}	Storage Temperature Range	-55 to 150	°C

PIN CONNECTION

PLCC44



PowerSO36



PIN FUNCTIONS

Pin #		Name	Description
PowerSO36	PLCC44		
1, 36	10-14	BRIDGE 1-POWER GND	Ground connection. They also conduct heat from die to printed circuit copper.
2, 17	15, 31	PH_1, PH_2	These TTL compatible logic inputs set the direction of current flow through the load. A high level causes current to flow from OUTPUT A to OUTPUT B.
3	16	COMP_IN_1	Negative input of error amplifier (1)
4	18	COMP_OUT_1	Error amplifier output (1)
5, 33	19, 7	OUT1A, OUT1B	Bridge 1 output connection
34	8	SENSE 1B	Positive input of the transconductance input amplifier (1)
6	20	Bridges DISABLE	Disables the bridges for additional safety during switching. When not connected the bridges are enabled
7	21	FREF (TRI_cap)	Triangle wave generation circuit capacitor. The value of this capacitor defines the output switching frequency
8	22	VCC (5V)	Supply Voltage Input for logic circuitry
9	23	POWER (Cherge Pump) GND	Ground connections of the internal charge pump circuit
10	24	VCP1	Charge pump oscillator output
11	25	VCP2	Input for external charge pump capacitor
12	26	VBOOT	Overvoltage input for driving of the upper DMOS
13, 31	27, 5	VS2, VS1	Supply voltage input for output stage
14, 22	28, 40	OUT2A, OUT2B	Bridge 2 output connection
21	38	SENSE 2B	Positive input of the transconductance input amplifier (2)
15	29	COMP_OUT_2	Error amplifier output (2)
16	30	COMP_IN_2	Negative input of error amplifier (2)
18-19	32-36	BRIDGE2 - POWER GND	Ground connection. They also conduct heat from die to printed circuit copper
20, 35	37, 9	SENSE 2A, SENSE 1A	Negative input of the transconductance input amplifier (2, 1)
23	41	I2_2	Logic input of the internal DAC (2). The output voltage of the DAC is a percentage of the VRef voltage applied according to the truth table of page 7
24	42	I1_2	See pin 23
25	43	I0_2	See pin 23
26, 28	44, 2	VREF2, VREF1	Reference voltages for the internal DACs, determining the output current value. Output current also depends on the logic inputs of the DAC and on the sensing resistor value
27	1	SIGNAL GND	Signal ground connection
29	3	I0_1	Logic input of the internal DAC (1). The output voltage of the DAC is a percentage of the Vref voltage applied according to the thruth table of page 7
30	4	I1_1	See pin 29
32	6	I2_1	See pin 29
	17, 39	N.C.	Pins not connected.

THERMAL DATA

Symbol	Parameter	PSO36	PLCC44	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction Ambient	17(*)	37(**)	°C

(*) Mounted on aluminum substrate.

(**) Mounted on heatsink 5x5 sqm, thickness: 35µm.

ELECTRICAL CHARACTERISTICS (V_S = 42V; V_{CC} = 5V; V_{boot} = 52V; T_j = 25°; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		10		45	V
V_{CC}	Logic Supply Voltage		4.75		5.25	V
V_{Sense}	Max Drop Across Sense Resistor				1.25	V
$I_{S(on)}$	V_S Quiescent Current	Both bridges ON, No Load		TBD		mA
$I_{S(off)}$	V_S Quiescent Current	Both bridges OFF		TBD		mA
$I_{CC\ (OFF)}$	V_{CC} Quiescent Current	DISABLE = LOW		TBD		mA
$I_{CC\ (ON)}$	VCC Quiescent Current	DISABLE = HIGH		TBD		mA
$T_{h\text{-}SD}$	Shut Down Temperature		135	160		°C
$T_{h\text{-}SD\text{-}H}$	Shut Down Hysteresis			25		°C
T_J	Thermal Shutdown			170		°C
T_d	Delay Time Protection			500		ns
f_{osc}	Triangular Oscillator Frequency	C_{FREF} = 1nF		20		KHz
DC	Output Duty Cycle		0		100	%
TRANSISTORS						
IDSS	leakage Current	OFF			500	µA
$R_{ds(on)}$	On Resistance	ON		0.6	0.75	Ω
V_f	Flywheel diode Voltage	If =1.0A		1.2	1.6	V
CONTROL LOGIC						
$V_{in(H)}$	Input Voltage	All Inputs	2		V_{CC}	V
$V_{in(L)}$	Input Voltage	All Inputs	0		0.8	V
$I_{in(H)}$	Input Current (Note 1)	V_{in} = 2V			10	µA
$I_{in(L)}$	Input Current	V_{in} = 0.8V	-150			µA
$I_{in(H)}$	Disable Pin Input Current	Vin = 2V			150	µA
V_{ref}	Reference Voltage	operating	0		2.5	V
I_{ref}	V_{ref} Terminal Input Current	Input = 500mV	-2		2	µA
$\frac{I_{LOAD}}{I_{MAX}}$ (%)	Output Current Levels (at trip point)	$I_2 = I_1 = I_0 = H$		no Current		%
		$I_2 = I_1 = H, I_0 = L$		19.4		%
		$I_2 = I_0 = H, I_1 = L$		38.7		%
		$I_0 = I_1 = L, I_2 = H$		54.8		%
		$I_0 = I_1 = H, I_2 = L$		71		%
		$I_0 = I_2 = L, I_1 = H$		83.9		%
		$I_1 = I_2 = L, I_0 = H$		93.5		%
		$I_0 = I_1 = I_2 = L$		100		%
V_{ref}/V_{sense}	PWM Loop Transfer Ratio			2		V

Note 1: This is true for all the logic inputs except the disable input.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SENSE AMPLIFIER						
V_{cm}	Input Common Mode Voltage Range		-0.7		V_S+0.7	V
I_{inp}	Input Bias			TBD		µA
ERROR AMPLIFIER						
V_{OS}	Input Offset Voltage		-5		+5	mV
I_b	Input Bias Current			TBD		nA
G_V	Open Loop Voltage Gain		80			dB
SR	Output Slew Rate		0.6			V/µs
GBW	Gain Bandwidth Product		1			MHz
PSRR	Power supply rejection ratio		80			dB
V_O	Output Voltage Swing			TBD		V
CHARGE PUMP						
C_{BOOT}	Storage capacitor			100		nF
V_{BOOT}	Storage Voltage		V_S+6		V_S+12	V
C_P	Pump Capacitor			10		nF

FUNCTIONAL DESCRIPTION

The circuit is intended to drive both windings of a bipolar stepper motor or two DC motors.

The current control is generated through a switch mode regulation.

With this system the direction and the amplitude of the load current are depending on the relation of phase and duty cycle between the two outputs of the current control loop.

The L6258 power stage is composed by power DMOS in bridge configuration like that of figure 1, where the bridge outputs OUTA and OUTB are driven to Vs with an high level at the inputs INA and INB while are driven to ground with a low level at the same inputs .

The zero current condition is obtained by driving the two half bridge with the two signals INA and INB having the same phase and 50% of duty cycle.

In this case the outputs of the two half bridges are continuously switched between Vs power supply and ground, but keeping the differential voltage across the load equal to zero.

In figure 1A, is shown the timing diagram of the two outputs behaviour and the load current of the circuit in figure 1 in the case of this working condition.

Following will be considered positive the current flowing into the load with a direction from OUTA to OUTB, while will be considered negative the current flowing into load with a direction from OUTB to OUTA.

Now just increasing the duty cycle of the INA signal and decreasing that of the INB signal we drive positive current into the load.

Being the two outputs in this way no more in phase, the current can flow into the load trough the bridge diagonal formed by T1 and T4 when the output OUTA is driven to Vs and the output OUTB is driven to ground, while there will be a current recirculation into the higher side of the bridge, through T1 and T2, when both the outputs are at Vs and a current recirculation into the lower side of the bridge, through T3 and T4, when both the outputs are at ground.

As the voltage applied to the load for recirculation is low, the resulting current discharge time constant is higher than the current charging time constant during the period in which the current flows into the load through the bridge diagonal formed by T1 and T4. In this way the load current will be positive with an average amplitude depending on the difference in duty cycle of the two driving signals.

In figure 1B is shown the timing diagram in the case of positive load current

On the contrary, if we want to drive negative current into the load is necessary to decrease the duty cycle of the INA signal and increase that of the INB signal. In this way we obtain a phase shift between the two outputs such to have current flowing into the bridge diagonal formed by T2 and T3 when the output OUTA is driven to ground and output OUTB is driven to Vs, while we will have

the same current recirculation conditions of the previous case when both the outputs are driven to Vs or to ground.

So, in this case the load current will be negative with an average amplitude always depending by the difference in duty cycle of the two driving signals.

In figure 1C is shown the timing diagram in the case of negative load current .

Figure 2 shows the device block diagram of the complete current control loop.

Figure 1.

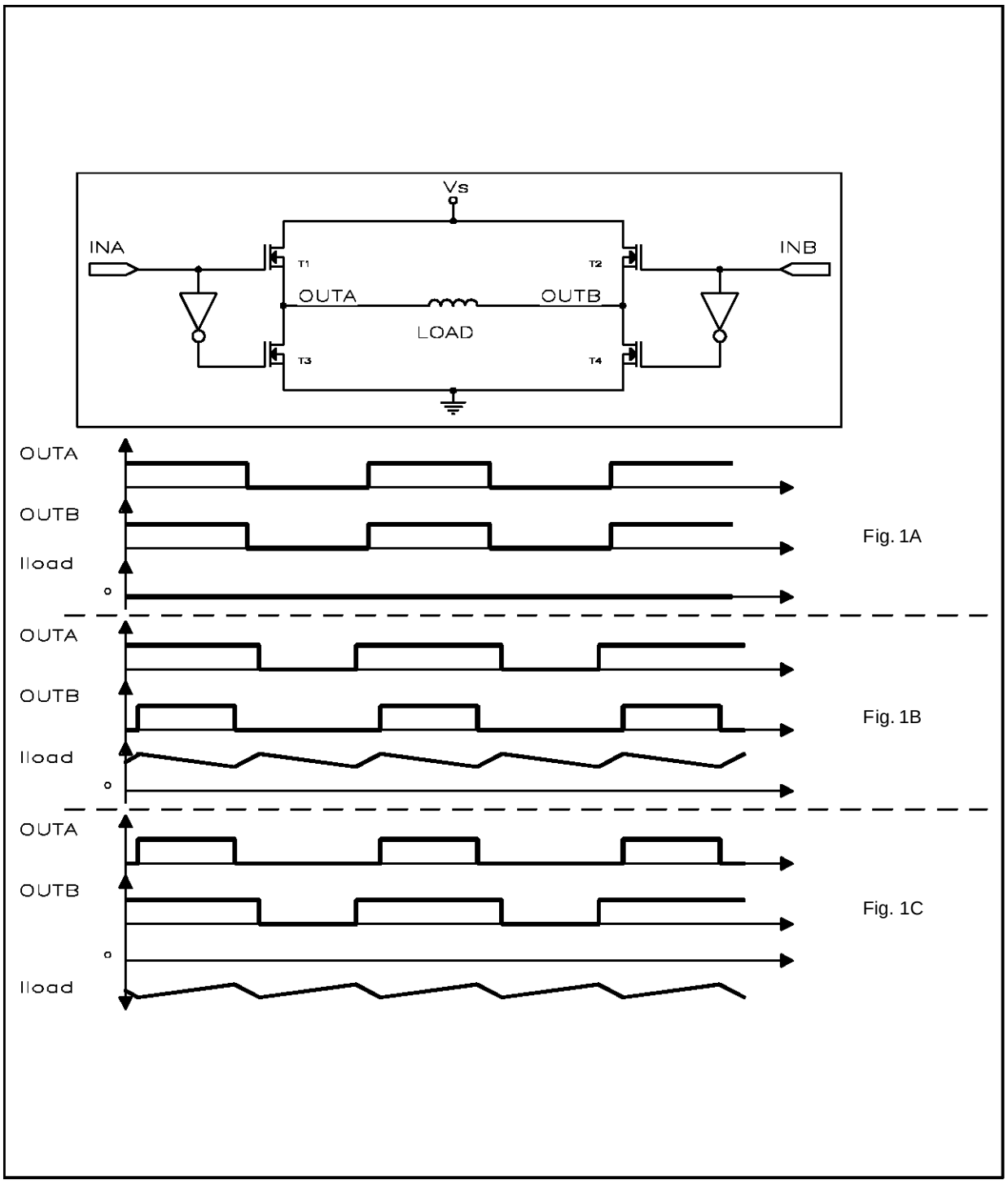
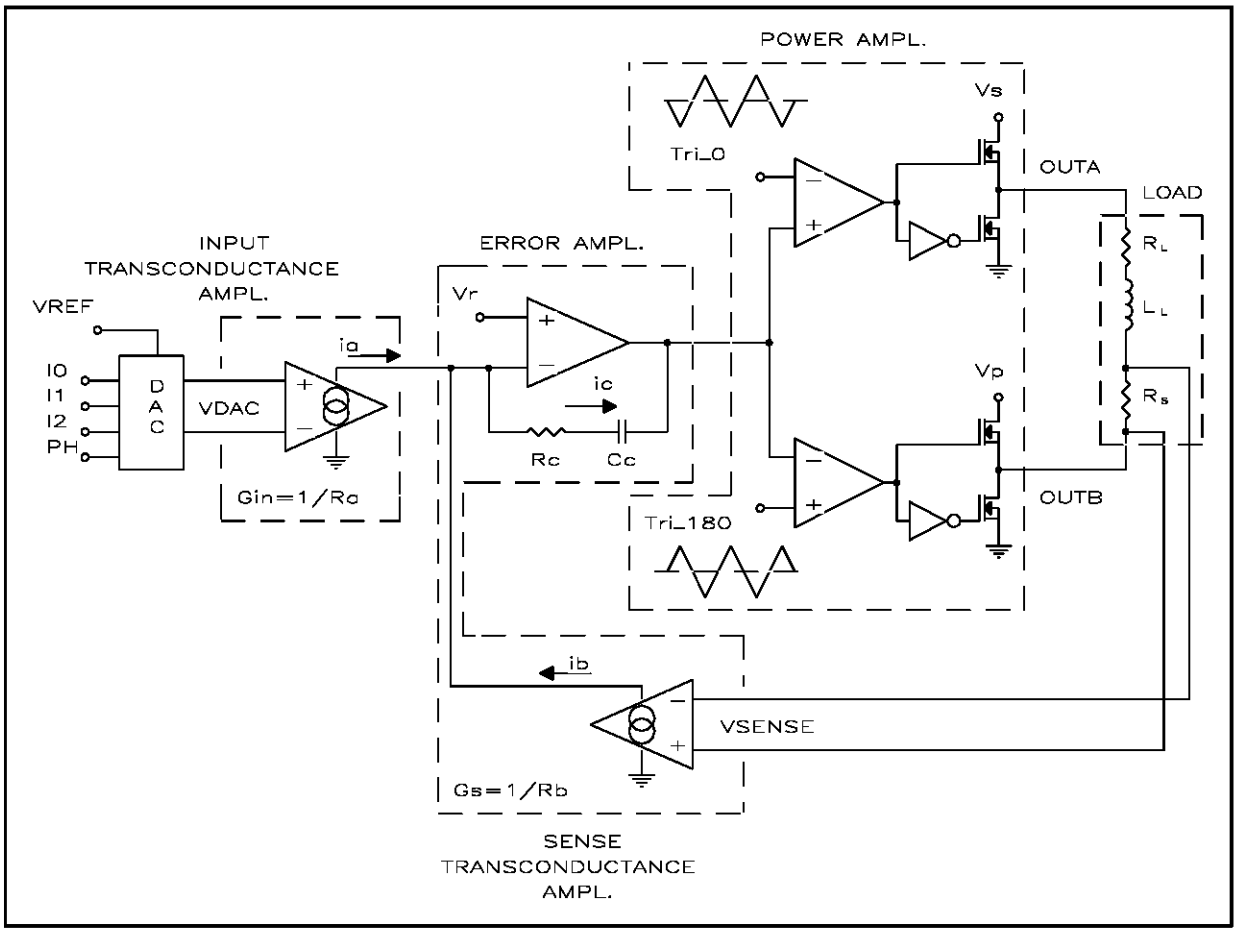


Figure 2.



REFERENCE VOLTAGE

The voltage applied to VREF pin is the reference for the internal DAC and, together with the sense resistor value, defines the maximum current into the motor winding according to the following relation:

$$I_{MAX} = \frac{0.5 \cdot V_{REF}}{R_S}$$

INPUT LOGIC (I0 - I1 - I2)

The current level in the motor winding is selected according to this table:

I2	I1	I0	Current level % of I_{MAX}
H	H	H	No Current
H	H	L	19.4
H	L	H	38.7
H	L	L	54.8
L	H	H	71
L	H	L	83.9
L	L	H	93.5
L	L	L	100

PHASE INPUT (PH)

The logic level applied to this input determines the direction of the current flowing in the winding of the motor.

High level on the phase input causes the motor current flowing from OUTA through the winding to OUTB.

TRIANGLE GENERATOR

This circuit generates the two triangle waves TRI_0 and TRI_180 internally used to generate the duty cycle variation of the signals driving the output stage in bridge configuration.

The frequency of the triangle wave defines the switching frequency of the output, and can be adjusted by changing the capacitor connected at FREF pin :

$$F_{ref} = \frac{K}{C}$$

where : $K = 2 \times 10^{-5}$

CHARGE PUMP CIRCUIT

To ensure the correct driving of the high side drivers a voltage higher than Vs is supplied on the Vboot pin. This boostrap voltage is not needed for the low side power DMOS transistors because their sources terminals are grounded. To produce this voltage a charge pump method is used and made by using two external capacitors; one connected to the internal oscillator and the other to storage the overvoltage needed for the driving the gates of the high side DMOS.

CURRENT CONTROL LOOP

The current control loop is a tranconductance amplifier working in PWM mode.

The motor current is a function of the programmed DAC voltage.

To keep under control the output current, the current control modulates the duty cycle of the two outputs OUTA and OUTB, and a sensing resistor Rs is connected in series with the motor winding in order to produce a voltage used as feedback to be compared with the programmed voltage of the DAC .

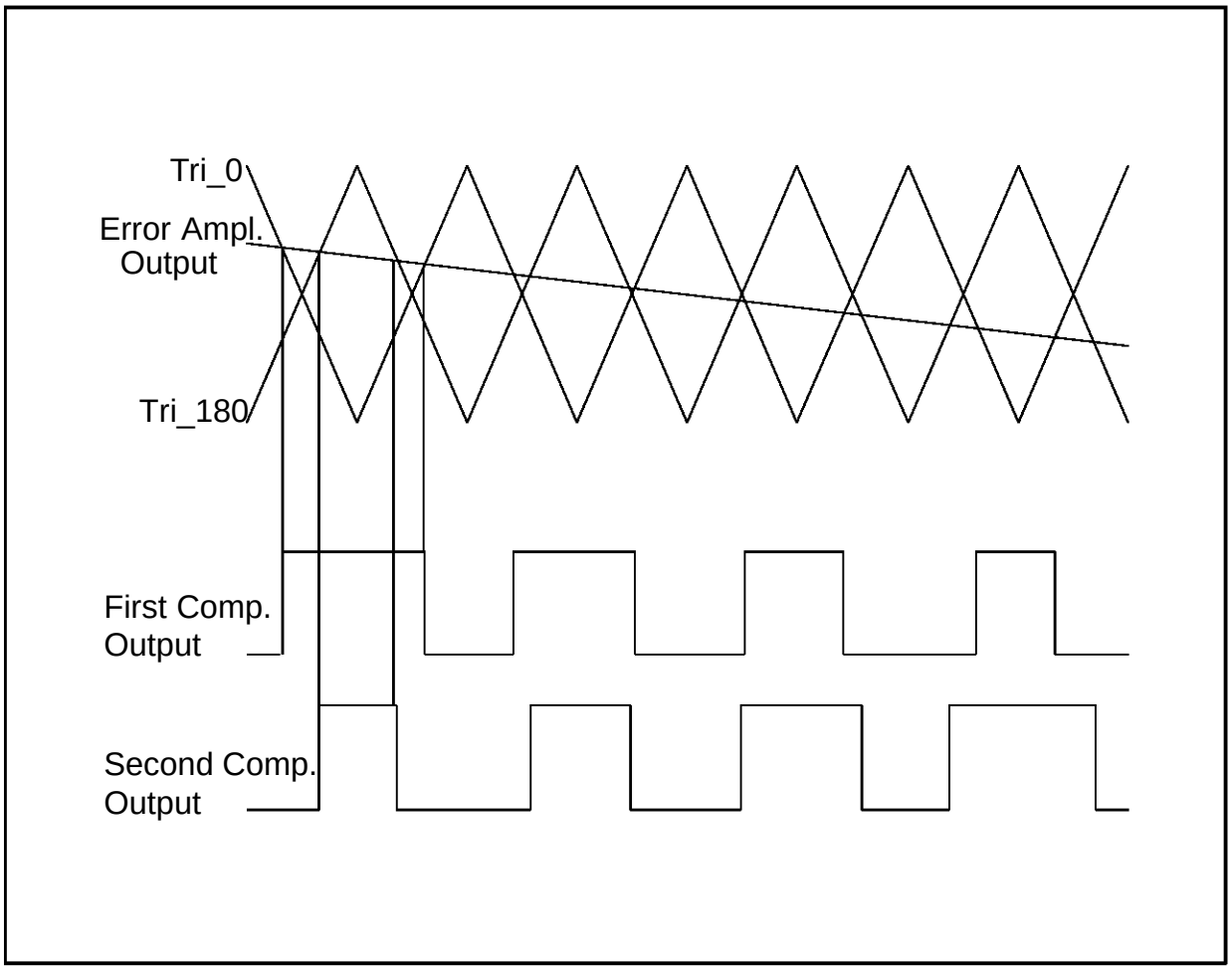
The duty cycle modulation of the two outputs is generated by the comparison between the voltage at the output of the error amplifier, with two triangle wave references .

In order to drive the output bridge with the duty cycle modulation explained before, the signals driving each output (OUTA & OUTB) are generated by the use of the two comparators having as reference two triangle wave signals Tri_0 and Tri_180 of the same amplitude, the same average value (in our case Vr), but with a 180° of phase shift each other.

The two triangle wave references are respectively applied to the inverting input of the first comparator and to the non inverting input of the second comparator .

The other two inputs of the comparators are connected together to the error amplifier output voltage resulting by the difference between the programmed DAC voltage and the voltage across the sensing resistor (see fig. 3).

Figure 3.



In the case of VDAC equal to zero, the transconductance loop is balanced at the value of Vr, so the outputs of the two comparators are signals having the same phase and 50% of duty cycle .

Being the output bridge driving signals in phase with 50% of duty cycle, the two outputs OUTA and OUTB are simultaneously driven from Vs to ground ; the resulting differential voltage across the load in this case is zero and no current will flow in the motor winding.

With positive differential voltage VDAC, the transconductance loop will be positively unbalanced respected Vr.

In this case being the error amplifier output voltage greater than Vr, the output of the first comparator is a square wave with a duty cycle higher than 50%, while the output of the second comparator is a square wave with a duty cycle lower than 50%.

The variation in duty cycle obtained at the outputs of the two comparators is of the same entity, but one in positive and the other in negative respected the 50% level.

The two driving signals, generated in this case, drive the two outputs in such a way to have switched current flowing from OUTA through the motor winding to OUTB.

With negative differential voltage VIN, the transconductance loop will be negatively unbalanced respected Vr.

In this case the output of the first comparator is a square wave with a duty cycle lower than 50%, while the output of the second comparator is a square wave with a duty cycle higher than 50%.

The variation in duty cycle obtained at the outputs of the two comparators is always of the same entity.

The two driving signals, generated in this case, drive the the two outputs in such a way to have switched current flowing from OUTB through the motor winding to OUTA.

CURRENT CONTROL LOOP COMPENSATION

In order to have a flexible system able to drive motors with different electrical characteristics, the non inverting input (COMP_IN) and the output of the error amplifier (COMP_OUT) are available.

Connecting at these pins an external RC compensation network it is possible to adjust the gain and the bandwidth of the current control loop.

L6258 - PWM CURRENT CONTROL LOOP

OPEN LOOP TRANSFER FUNCTION ANALYSIS

Block diagram : please refer to Fig. 2.

Application data:

V_S = 24V	Gs transconductance gain = 1/Rb
L_L = 12mH	Gin transconductance gain = 1/Ra
R_L = 12Ω	Ampl. of the Tria_0_180 ref. = 1.6V (peak to peak)
R_S = 0.33Ω	R_a = 40KΩ
R_C = to be calculated	R_b = 20KΩ
C_C = to be calculated	Vr = Internal reference equal to V_{CC}/2 (Typ. 2.5V)

these data refer to a typical application, and will be used as an example during the analysis of the stability of the current control loop.

The block diagram shows the schematics of the L6258 internal current control loop working in PWM mode; the current into the load is a function of the input control voltage VDAC , and the relation between the two variables is given by the following formula:

$$I_{load} \cdot R_S \cdot G_S = VDAC \cdot G_{in}$$

$$I_{load} \cdot R_S \cdot \frac{1}{R_B} = VDAC \cdot \frac{1}{R_a}$$

$$I_{load} = VDAC \cdot \frac{R_b}{R_a \cdot R_S} = 0.5 \cdot \frac{VDAC}{R_S} \quad (A)$$

where:

VDAC	is the control voltage defining the load current value
G_{in}	is the gain of the input transconductance amplifier ($1/R_a$)
G_s	is the gain of the sense transconductance amplifier ($1/R_b$)
Rs	is the resistor connected in series to the output to sense the load current

In this system the input voltage is compared with the feedback voltage coming from the sense resistor, then the difference between this two signals is amplified by the error amplifier in order to have an error signal controlling the duty cycle of the output stage keeping the load current under control.

It is clear that to have a good performance of the current control loop, the error amplifier must have an high DC gain and a large bandwidth .

Gain and bandwidth must be chosen depending on many parameters of the application, like the characteristics of the load, power supply etc..., and most important is the stability of the system that must always be guaranteed.

To have a very flexible system and to have the possibility to adapt the system to any application, the error amplifier must be compensated using an

RC network connected between the output and the negative input of the same.

For the evaluation of the stability of the system, we have to consider the open loop gain of the current control loop:

$$Aloop = ACerr \cdot ACpw \cdot ACload \cdot ACsense$$

where AC... is the gain of the blocks that refers to the error, power and sense amplifier plus the attenuation of the load block.

The same formula in dB can be written in this way:

$$Aloop|_{dB} = ACerr|_{dB} + ACpw|_{dB} + ACload|_{dB} + ACsense|_{dB}$$

So now we can start to analyse the dynamic characteristics of each single block, with particular attention to the error amplifier.

POWER AMPLIFIER :

The power amplifier is not a linear amplifier, but is a circuit driving in PWM mode the output stage in full bridge configuration.

The output duty cycle variation is given by the comparison between the voltage of the error amplifier and two triangle wave references Tri_0 and Tri_180. Because all the current control loop is referred to the Vr reference, the result is that when the output voltage of the error amplifier is equal to the Vr voltage the two output OutA and OutB have the same phase and duty cycle at 50%; increasing the output voltage of the error amplifier above the Vr voltage, the duty cycle of the OutA increases and the duty cycle of the OutB decreases of the same percentage; at the contrary decreasing the voltage of the error amplifier below the Vr voltage, the duty cycle of the OutA decreases and the duty cycle of the OutB increases of the same percentage.

The gain of this block is defined by the amplitude of the two triangle wave references; more precisely the gain of the power amplifier block is a reversed proportion of the amplitude of the two references.

In fact a variation of the error amplifier output voltage produces a larger variation in duty cycle of the two outputs OutA and OutB in case of low amplitude of the two triangle wave references.

The duty cycle has the max value of 100% when the input voltage is equal to the amplitude of the two triangle references.

The transfer function of this block consist in the relation between the output duty cycle and the amplitude of the triangle references.

$$V_{out} = 2 \cdot V_S \cdot (0.5 - DutyCycle)$$

$$ACpw|_{dB} = 20 \cdot \log\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{2 \cdot V_S}{\text{Triangle Amplitude}}$$

$$ACpw|_{dB} = 20 \cdot \log\frac{2 \cdot 24}{1.6} = 29.5dB$$

Moreover, having the two references Tri_0 and Tri_180 a triangular shape it is clear that the transfer function of this block is a linear constant gain without poles and zeros.

LOAD :

The load block is composed by the equivalent circuit of the motor winding (resistance and inductance) plus the sense resistor.

Note : the effect of the Bemf voltage of the motor will be considered later.

The input of this block is the PWM voltage of the power amplifier and as output we have the voltage across the sense resistor produced by the current flowing into the motor winding. The relation between the two variable is :

$$V_{sense} = \frac{V_{out}}{R_L + R_S} \cdot R_S$$

so the gain of this block is:

$$ACload = \frac{V_{sense}}{V_{out}} = \frac{R_S}{R_L + R_S}$$

$$ACload|_{dB} = 20 \cdot \log\frac{R_S}{R_L + R_S}$$

$$ACload|_{dB} = 20 \cdot \log\frac{0.33}{12 + 0.33} = -31.4dB$$

where:

RL is the equivalent resistance of the motor winding

RS is the sense resistor

Because of the inductance of the motor LL, the load has a pole at a frequency :

$$Fpole = \frac{1}{2\pi \cdot \frac{L_L}{R_L + R_S}}$$

$$Fpole = \frac{1}{6.28 \cdot \frac{12 \cdot 10^{-3}}{12 + 0.33}} = 163Hz$$

Before analysing the error amplifier block and the sense transconductance block, let's do this con-

sideration :

$Aloop|_{dB} = Ax|_{dB} + Bx|_{dB}$

$Ax|_{dB} = ACpw|_{dB} + ACload|_{dB}$

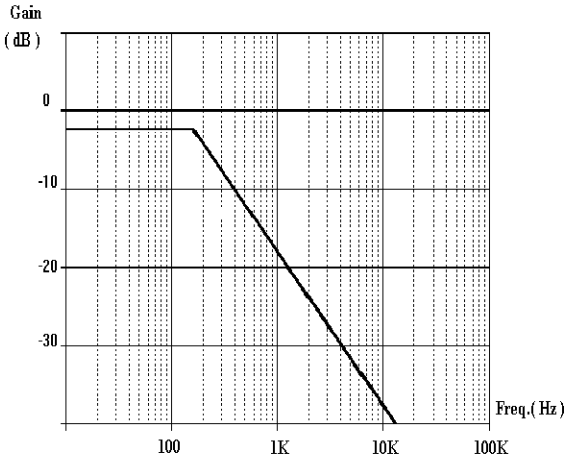
and

$Bx|_{dB} = ACerr|_{dB} + ACsense|_{dB}$

this means that $Ax|_{dB}$ is the sum of the power amplifier and load blocks;

$Ax|_{dB} = (29,5) + (-31.4) = -1.9dB$

The BODE analysis of the transfer function of Ax is:



The Bode plot of the $Ax|_{dB}$ function shows a DC gain of -1.9dB and a pole at 163Hz.

It is clear now that because of the negative gain of the Ax function, Bx function must have an high DC gain in order to increment the total open loop gain increasing the bandwidth too.

ERROR AMPLIFIER and SENSE AMPLIFIER:

As explained before the gain of these two blocks is :

$Bx|_{dB} = ACerr|_{dB} + ACsense|_{dB}$

Being the voltage across the sense resistor the input of the Bx block and the error amplifier voltage the output of the same, the voltage gain is given by :

$$ib = Vsense \cdot Gs = Vsense \cdot \frac{1}{Rb}$$

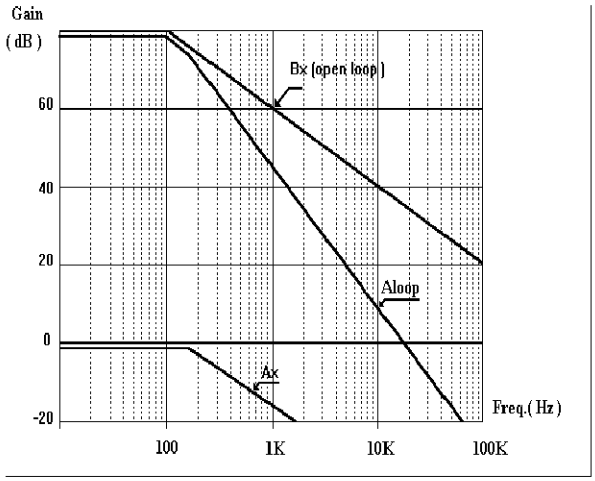
$$Verr\_out = -(ic \cdot Zc) \text{ so } \quad ic = -(Verr\_out \cdot \frac{1}{Zc})$$

because ib = ic we have:

$$Vsense \cdot \frac{1}{Rb} = -(Verr\_out \cdot \frac{1}{Zc})$$

$$Bx = -\frac{Verr\_out}{Vsense} = -\frac{Zc}{Rb}$$

In the case of no external RC network is used to compensate the error amplifier, the typical open loop transfer function of the error plus the sense amplifier is something with a gain around 80dB and a unity gain bandwidth at 1MHz. In this case the situation of the total transfer function Aloop, given by the sum of the Ax|dB and Bx|dB is :



The BODE diagram shows together the error amplifier open loop transfer function, the Ax function and the resultant total Aloop given by the following equation :

$Aloop|_{dB} = Ax|_{dB} + Bx|_{dB}$

The total Aloop has an high DC gain of 78.1dB with a bandwidth of 15KHz, but the problem in this case is the stability of the system; in fact the total Aloop cross the zero dB axis with a slope of -40dB/decade.

It is necessary then to compensate the error amplifier in order to obtain a total Aloop with an high DC gain and a large bandwidth and specially with enough phase margin to guarantee the stability of the system.

A method to reach the stability of the system, using the RC network showed in the block diagram, is to cancel the load pole with the zero given by the compensation of the error amplifier.

The transfer function of the Bx block with the compensation on the error amplifier is :

$$Bx = -\frac{Zc}{Rb} = -\frac{Rc - j\frac{1}{2\pi \cdot f \cdot Cc}}{Rb}$$

So in this case the Bx block has a DC gain equal to the case in open loop and a zero at a frequency given by the following formula :

$$Fzero = \frac{1}{2\pi \cdot Rc \cdot Cc}$$

In order to cancel the pole of the load, the zero of the Bx block must be located at the same frequency of 163Hz; so now we have to find a compromise between the resistor and the capacitor of the compensation network.

Considering that the resistor value defines the gain of the Bx block at the zero frequency, it is clear that this parameter will influence the total bandwidth of the system because, annulling the load pole with the error amplifier zero, the slope of the total transfer function is -20dB/decade.

So the resistor value must be chosen in order to have an error amplifier gain enough to guarantee a desired total bandwidth .

In our example we fix the gain of the Bx block at zero frequency at 35dB, so from the formula:

$$Bx\_gain_{@zero\ freq.} = 20 \cdot \log\frac{Rc}{Rb} \quad \text{where: } Rb = 20K\Omega$$

we have : $Rc = 1.1M\Omega$

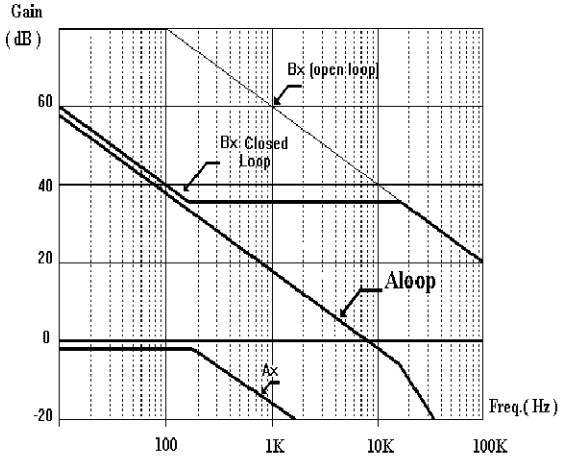
so to have the zero at 163Hz the capacitor must be :

$$Cc = \frac{1}{2\pi \cdot Fzero \cdot Rc} = \frac{1}{6.28 \cdot 163 \cdot 1.1 \cdot 10^6} = 880pF$$

Let's now analyse how is the new Aloop transfer function with a compensation network on the error amplifier .

The following bode diagram now shows :

- the Ax function showing the position of the load pole
- the open loop transfer function of the Bx block
- the transfer function of the Bx with the RC compensation network on the error amplifier
- the total Aloop transfer function that is the sum of the Ax function plus the transfer function of the compensated Bx block.

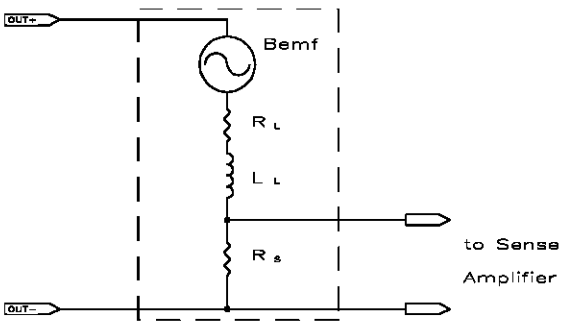


We can see that the effect of the load pole is annulled by the zero of the Bx block ; the total Aloop cross the 0dB axis with a slope of -20dB/decade, having in this way a stable system with an high gain at low frequency and a bandwidth of around 8KHz.

If now, for instance , we want to increase the bandwidth of the system, it is necessary to increase the gain of the Bx block, keeping the zero in the same position. In this way what we have is a shift of the total Aloop transfer function upside of a number of dB given by the difference between the new gain of the Bx block with the original gain of the example.

Effect of the Bemf of the stepper motor on the current control loop stability

In order to evaluate what is the effect of the Bemf voltage of the stepper motor we have to look at the load block :



The schematic now shows the equivalent circuit of the stepper motor including a sine wave voltage generator representing the Bemf of the same. The Bemf voltage of the motor is not a constant, but is a variable that changes the value depending on the speed of the motor.

Increasing the motor speed the Bemf voltage increases :

$Bemf = Kt \cdot \omega$

where:

Kt is the motor constant

ω is the motor speed in radiant per second

The formula defining the gain of the load considering the Bemf of the stepper motor becomes:

$$ACload = \frac{Vsense}{Vout} = \frac{(V_S - Bemf) \cdot \frac{R_S}{R_L + R_S}}{V_S}$$

$$ACload = \frac{V_S - Bemf}{V_S} \cdot \frac{R_S}{R_L + R_S}$$

$$ACload|_{dB} = 20 \cdot \log\left(\frac{V_S - Bemf}{V_S} \cdot \frac{R_S}{R_L + R_S}\right)$$

we can see that the Bemf influences only the gain of the load block and does not introduce any additional poles or zeros, so from the stability point of view the effect of the Bemf of the motor is not critical because the phase margin remains the same.

Practically the only effect of the Bemf is to limit the gain of the total Aloop with a consequent variation of the bandwidth of the system.

APPLICATION INFORMATION

A typical application circuit is shown in Fig.4.

INTERFERENCE

As the circuit operates with switch mode current regulation, to reduce the effect of the wiring inductance a good capacitor (100nF) can be placed on the board near the package, between the power supply line (pin 13,31) and the power ground (pin 1,36,18,19) to absorb the small amount of inductive energy in the leads..

It should be noted that this capacitor is usually required in addition to an electrolytic capacitor, which has poor performance at high frequencies, always located near the package, between power supply voltage (pin 13,31) and power ground (pin 1,36,18,19) to have a current recirculation path during the fast current decay or during the phase change.

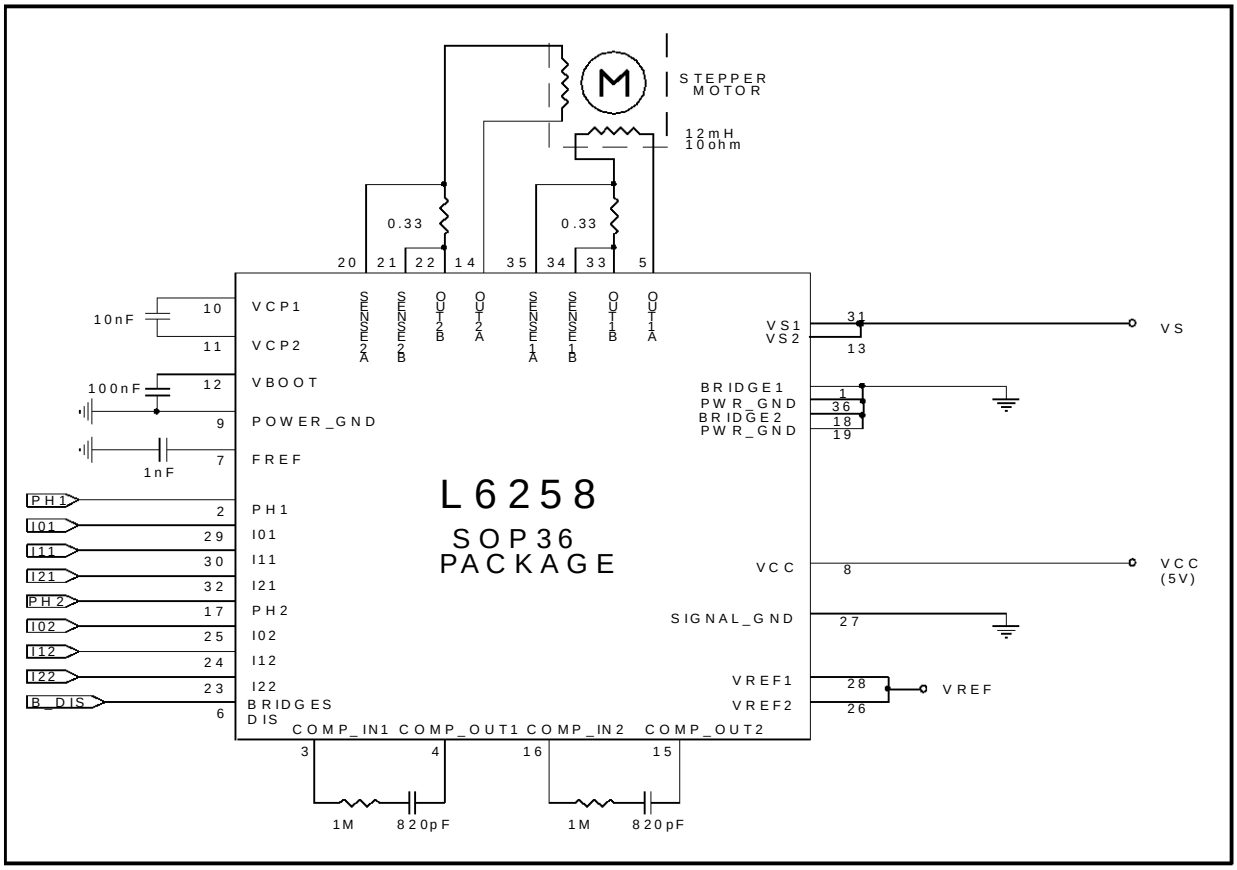
The range value of this capacitor is between some uF and 100uF, and anyway must be chosen depending on application parameters like the motor inductance and load current amplitude.

A decoupling capacitor of 100nF is suggested also between the logic supply and ground.

A non inductive resistor is the best way to implement the sensing, but when that is not possible, more metal film resistor of the same value can be paralleled.

The two inputs for the sensing of the winding motor current (SENSE_A & SENSE_B) should be connected directly on the sensing resistor Rs terminals, and the path lead between the Rs and the two sensing inputs should be kept as short as possible.

Figure 4: Typical Application Circuit.



APLLICATION INFORMATION (continued)

MOTOR SELECTION

Some stepper motor have such high core losses that they are not suited for switch mode current regulation. Also, some stepper motors are not designed for continuous operation at maximum current. As the circuit can drive a constant current through the motor, its temperature might increase exceedingly both at low and high speed operation.

UNUSED INPUTS

Unused inputs should be connected to the proper voltage levels in order to get the highest noise immunity.

NOTES ON PCB DESIGN

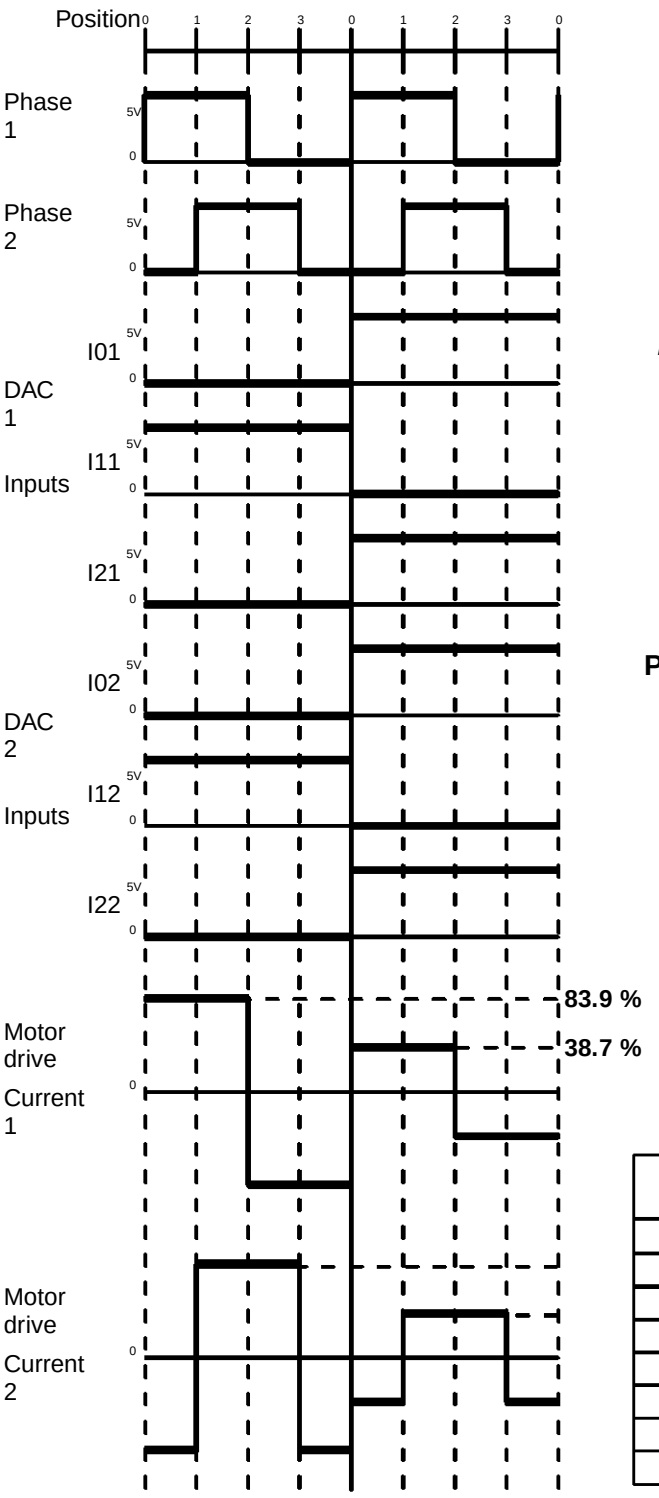
We recommend to observe the following layout rules to avoid application problems with ground and anomalous recirculation current.

The by-pass capacitors for the power and logic supply must to be kept as close to the IC as possible.

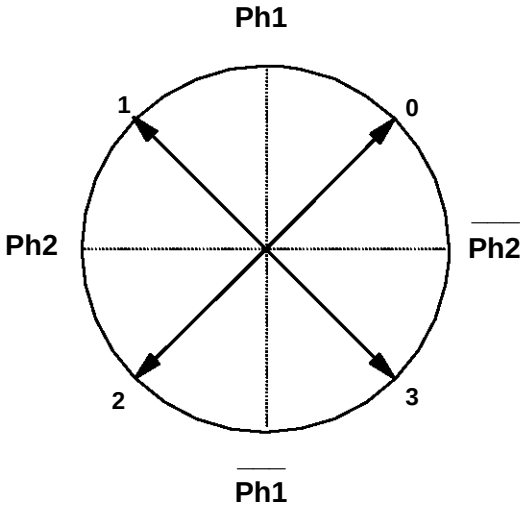
It's important to separate on the PCB board the logic and power grounds and the internal charge pump circuit ground avoiding that ground traces of the logic signals cross the ground traces of the power signals.

Because the IC uses the board as a heat sink, the dissipating copper area must be sized in accordance with the required value of $R_{thj\text{-}amb}$.

Figure 5: Full step operation mode timing diagram (Phase - DAC input and Motor Current)

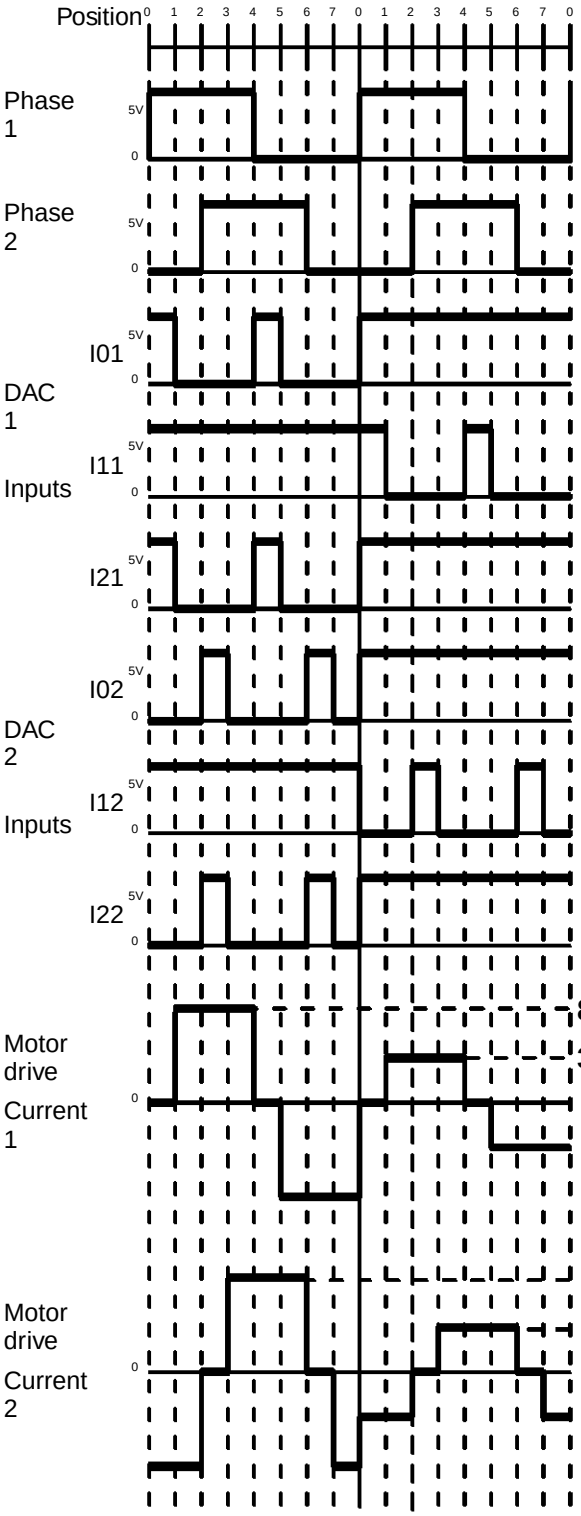


Full Step Vector

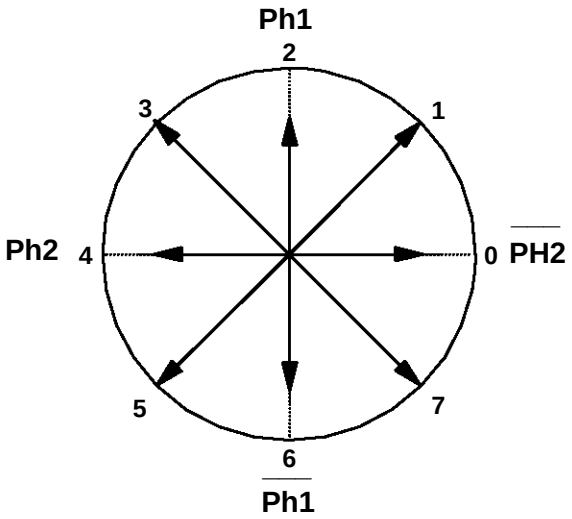


I2	I1	I0	Imax (%)
L	L	L	100
L	L	H	93.5
L	H	L	83.9
L	H	H	71.0
H	L	L	54.8
H	L	H	38.7
H	H	L	19.4
H	H	H	0

Figure 6: Half step operation mode timing diagram (Phase - DAC input and Motor Current)

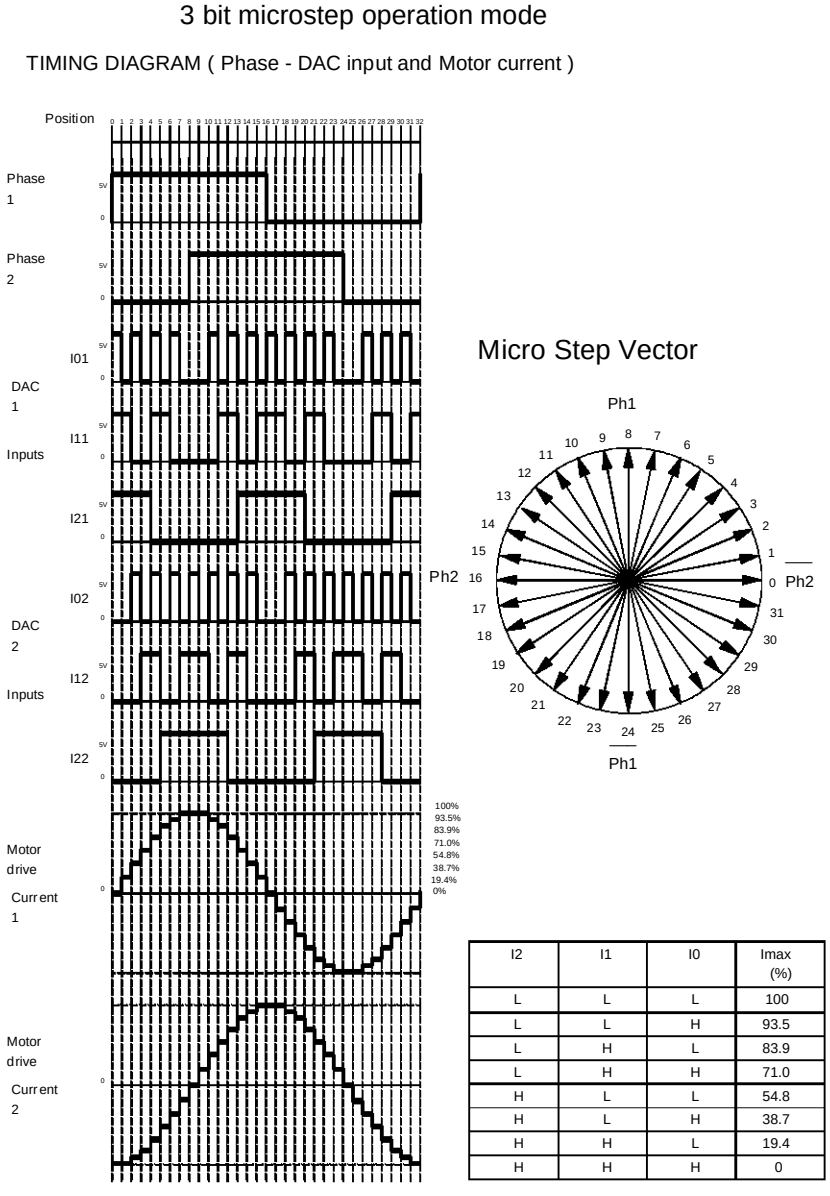


Half Step Vector



I2	I1	I0	Imax (%)
L	L	L	100
L	L	H	93.5
L	H	L	83.9
L	H	H	71.0
H	L	L	54.8
H	L	H	38.7
H	H	L	19.4
H	H	H	0

Figure 7: 3 bit microstep operation mode timing diagram (Phase - DAC input and Motor Current)

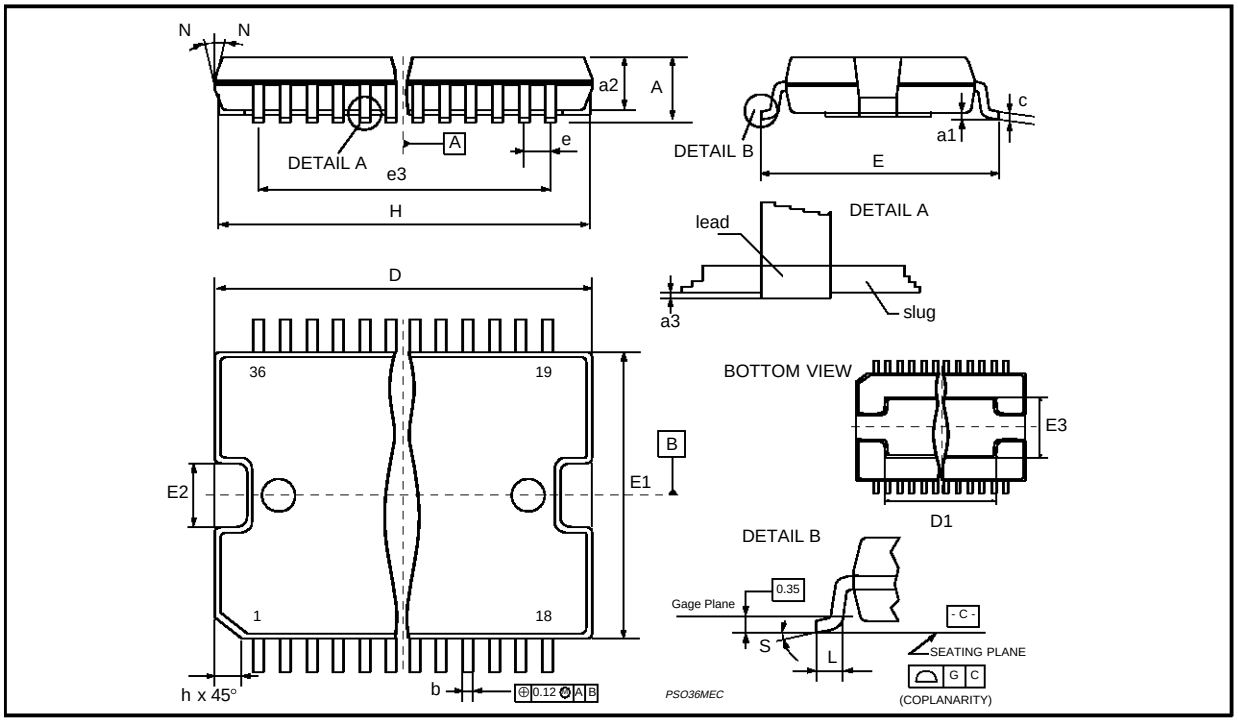


I2	I1	I0	Imax (%)
L	L	L	100
L	L	H	93.5
L	H	L	83.9
L	H	H	71.0
H	L	L	54.8
H	L	H	38.7
H	H	L	19.4
H	H	H	0

PowerSO36 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.141
a1	0.10		0.30	0.004		0.012
a2			3.30			0.130
a3	0		0.10	0		0.004
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D (1)	15.80		16.00	0.622		0.630
D1	9.40		9.80	0.370		0.385
E	13.90		14.50	0.547		0.570
e		0.65			0.025	
e3		11.05			0.435	
E1 (1)	10.90		11.10	0.429		0.437
E2			2.90			0.114
E3	5.80		6.20	0.228		0.244
G	0		0.10	0		0.004
H	15.50		15.90	0.610		0.626
h			1.10			0.043
L	0.80		1.10	0.031		0.043
N	10°(max.)					
S	8°(max.)					

(1): "D" and "E1" do not include mold flash or protrusions
-Mold flash or protrusions shall not exceed 0.15mm (0.006 inch)
Critical dimensions are "a3", "E" and "G".



PLCC44 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045